

PTO/SB/21 (08-00)

MODIFIED

AUG 10 2 2005 FORM			Application Number		09/920,240					
			Filing Date		08/01/2001					
			First Named Inve	ntor	Pierte ROO					
(to be used for all correspondence after initial filing) 213200.00072			Group Art Unit		2682					
213200.00072			Examiner Name		Eugene Yun					
Total Number of	ion 17	Attorney Docket N	MP0039.CIP							
ENCLOSURES (check all that apply)										
	claration(s) dequest ent Request ure Statement with ED REFERENCES iority g Parts/	Drawing Licensin Petition Petition Provisio Associat Termina Reques	nent Papers (pplication) (s) g-related Papers to Convert to a nal Application the Power of Attorney I Disclaimer t for Refund Interpret of CD(s)		After Allowance Communication to Group Appeal Communication to Board of Appeals and Interferences Appeal Communication to Group (Appeal Notice, Brief, Reply Brief) Proprietary Information Status Letter Other Enclosure(s) (please identify below):					
	SIGNATURE	E OF APPLI	CANT, ATTORNEY	, OR A	GENT					
Firm or Individual name Andrew J. Bateman Registration No.: 45,573 Signature										
Date			08/02/20	05						
CERTIFICATE OF MAILING										
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231 on this date:										
Typed or printed name	•									
Signature				Date						

MP0039CIP Patent

AUG '0 2 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Pierte ROO

Application No.: 09/920,240

Filed: August 1, 2001

For: ACTIVE RESISTIVE SUMMER FOR

A TRANSFORMER HYBRID

Examiner: Eugene YUN

Group Art Unit: 2682

Confirmation No.: 4035

Date: August 2, 2005

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In compliance with the duty of disclosure under 37 CFR § 1.56 and the requirements of M.P.E.P. § 2001.06(c), and in accordance with the practice under 37 CFR §§ 1.97 and 1.98, the Examiner's attention is directed to the documents listed on the enclosed PTO-1449s and to copies of any literature and non-U.S. patent documents submitted herewith.

In accordance with 37 CFR § 1.97(h), this Information Disclosure Statement is not to be construed as an admission that the information cited is or is considered to be material to patentability as defined in 37 CFR § 1.56(b), nor as an admission that the information constitutes prior art within the meaning of 35 USC §§ 102 and/or 103.

It is respectfully requested that the information listed on the PTO-1449 be considered by the Examiner, and that an initialed copy of the PTO-1449 be returned indicating that such information was considered.

No fee is believed necessary for the submission of this Information Disclosure Statement. However, if deemed necessary, the Commissioner is authorized to charge the IDS fee of \$180.00 to Deposit Account No. 50-1710.

Should the Examiner have any questions, Applicant's undersigned attorney is reachable by telephone in our Washington, D.C. office at (202) 625-3547. The correspondence address of record is provided below.

IP Docket Katten Muchin Rosenman, LLP 1025 Thomas Jefferson St., NW East Lobby, Suite 700 Washington, DC 20007-5201 Facsimile No.: (202) 298-7570

Respectfully submitted, KATTEN MUCHIN ROSENMAN, LLP

Andrew J. Bateman Registration No. 45,573

FORM PTO 1449 MODIFIED U.S. PATENT AND TRADEMARK OFFICE					ATTORNEY DOCKET NO. APPLICATION NO.						
					MP0039.CIP		09/920,240				
LIST OF REFERENCES CITED BY APPLICANT					APPLICANT						
					Pierte ROO						
DATE SUBMITTED TO USPTO: August 2, 2005 AUG 10 2 2005					FILING DATE		GROUP				
					/2001	2	682				
FOREIGN PAT	TENT DOCUMENTS	2 200									
*EXAMINER INITIALS	DOCUMENT NUMBER	DOCUMENT NUMBER TRADEBATE		COUNTRY		SUBCLASS	TRANSLATION OR ABSTRACT				
						-					
OTHER DOCU	MENTS (Including author	<u> </u>	 nt pages, etc.)		<u> </u>		<u> </u>				
Gray, et al., ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS, pp 270 & 274.											
	Gray et al., Analysis	Gray et al., Analysis and Design of Analog Integrated Circuits, Fourth Edition, pp. 217-221.									
	Dally, et al., "Digital S	Dally, et al., "Digital Systems Engineering", cover and pgs. 390-391.									
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EXAMINER		DATE CONSID	PERED								
* EXAMINER: Initial if refe	erence considered, whether or not citation is in con	formance with MPEP 609; Draw line t	through citation if not in con	formance and not cons	idered, Include copy of th	is form with next communi	ication to applicant.				